Altera and Micron help propel HMC, but will 3D packaging limit interest?

Loring Wirbel - September 10, 2013

Altera Corp and Micron Technology Inc demonstrated a big step forward for Hybrid Memory Cube, by showing a Stratix V interface to the promising 3D technology. How might packaging limit HMC's popularity compared to special-purpose nonvolatiles like ferroelectric or magnetoresistive RAM?

In early August, we talked about the growing importance of memory and system-bus interfaces on next-generation FPGAs. Altera and Micron, both members of the HMC Consortium, are hoping to accelerate the viability and hence the utility of hybrid cubes by making them a mainstream alternative to DRAM and SRAM. Altera not only showed a Stratix V prototype, but indicated it would work on HMC for its upcoming Gen 10 family of FPGAs.

Developers of next-generation systems have looked for practical alternatives to volatile row-address/column-address memory types for decades. Some hoped for improved performance from specialized memories such as graphic RAMs or content-addressable memories. Others looked at exotic non-volatile memory ICs based on unique materials, including ferroelectric RAMs and magnetoresistive RAMs. An even more exotic nonvolatile is the phase-change chalcogenide memory, based on the work of Stanford Ovshinsky, and optimized by IBM and others. FRAMs and MRAMs have proven cost-effective in some mobile and embedded applications, but in general are unable to compete with mainstream high-speed RAM such as DDR3 and DDR4 devices.

Micron's work with the HMC Consortium takes into account the enormous strides made in 2.5D and 3D interconnect using through-hole vias and special substrates. In the new hybrid cube work, three-dimensional stacks of RAM are combined in one hybrid package with a substrate logic layer that forms an on-chip memory controller, using a packet protocol.

On the one hand, this maps with FPGA vendors' own plans. Altera, Xilinx, and some FPGA startups have indicated their interest in using a third dimension for logic interconnect, so a multi-layered hybrid will be commonplace in many future FPGAs, with or without unusual memories.

Still, one must recognize the learning curves for both foundries and designers. Large Asian foundries are becoming comfortable with 2.5D and 3D multilayer interconnect, so products moved into production in 2014 and 2015 should not carry a significant price premium over standard planar die. FPGA customers who are familiar with working with large ASICs or mixed-signal hybrids should not have a problem with devices like HMC memories. The height of the chip package is not as significant as the change in pinout, and this change in I/O pads is familiar with any type of hybrid device.

The Altera/Micron alliance could bring HMC over the viability hurdle. On the other hand, we've waited for years, sometimes decades, for some nonvolatile memories based on unique materials to move into high production. We're still waiting. Will the same be true for hybrid memories?

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