Hybrid Memory Cube Consortium Heralds 2013 as Turning Point for High-Performance Memory ICs, Gains Rapid Consensus for Final Specification and Decision to Renew Consortium

Collaboration Among 100 Developers and Adopters Will Enable New Disruptive Computing Solutions for Wide Range of Industrial to Consumer Segments

BOISE, Idaho and SEOUL, Korea (April 2, 2013) – More than 100 developer and adopter members of the Hybrid Memory Cube Consortium (HMCC) today announced they've reached consensus for the global standard that will deliver a much-anticipated, disruptive memory computing solution. Developed in only 17 months, the final specification marks the turning point for designers in a wide range of segments—from networking and high-performance computing, to industrial and beyond—to begin designing Hybrid Memory Cube (HMC) technology into future products.

A major breakthrough with HMC is the long-awaited utilization of advanced technologies to combine high-performance logic with state-of-the-art DRAM. With this first HMC milestone reached so quickly, consortium members have elected to extend their collaborative effort to achieve agreement on the next generation of HMC interface standards.

"The consensus we have among major memory companies and many others in the industry will contribute significantly to the launch of this promising technology." said Jim Elliott, Vice President, Memory Planning and Product Marketing, Samsung Semiconductor, Inc. "As a result of the work of the HMCC, IT system designers and manufacturers will be able to get new green memory solutions that outperform other memory options offered today."

"This milestone marks the tearing down of the memory wall," said Robert Feurle, Micron's Vice President for DRAM Marketing. "The industry agreement is going to help drive the fastest possible adoption of HMC technology, resulting in what we believe will be radical improvements to computing systems and, ultimately, consumer applications."

"HMC is a very special offering currently on the radar," said JH Oh, Vice President, DRAM Product Planning and Enabling Group, SK hynix Inc. "HMC brings a new level of capability to memory that provides exponential performance and efficiency gains that will redefine the future of memory."

As envisioned, HMC capabilities will leap beyond current and near-term memory architectures in the areas of performance, packaging and power efficiency.

One of the primary challenges facing the industry—and a key motivation for forming the HMCC—is that the memory bandwidth required by high-performance computers and next-generation networking equipment

has increased beyond what conventional memory architectures can efficiently provide. The term "memory wall" has been used to describe this challenge. Breaking through the memory wall requires an architecture such as HMC that can provide increased density and bandwidth with significantly lower power consumption.

The HMC standard focuses on alleviating an extremely challenging bandwidth bottleneck while optimizing the performance between processor and memory to drive high-bandwidth memory products scaled for a wide range of applications. The need for more efficient, high-bandwidth memory solutions has become particularly important for servers, high-performance computing, networking, cloud computing and consumer electronics.

The achieved specification provides an advanced, short-reach (SR) and ultra short-reach (USR) interconnection across physical layers (PHYs) for applications requiring tightly coupled or close-proximity memory support for FPGAs, ASICs and ASSPs, such as high-performance networking, and test and measurement. The next goal for the consortium is to further advance standards designed to increase data rate speeds from 10, 12.5 and 15 gigabits per second (Gb/s) up to 28 Gb/s for SR and from 10 Gb/s up to 15 Gb/s for USR. The next-generation specification is projected to gain consortium agreement by the first quarter of 2014.

The HMCC is a focused collaboration of OEMs, enablers and integrators who are cooperating to develop and implement an open interface standard for HMC. More than 100 leading technology companies from Asia, Japan, Europe and the U.S. have joined the effort, including Altera, ARM, Cray, Fujitsu, GLOBALFOUNDRIES, HP, IBM, Marvell, Micron Technology, National Instruments, Open-Silicon, Samsung, SK hynix, ST Microelectronics, Teradyne and Xilinx. Continued collaborations within the consortium could ultimately facilitate new uses in HPC, networking, energy, wireless communications, transportation, security and other semiconductor applications.

Additional information, technical support specifications and other tools for adopting the technology can be found at www.hybridmemorycube.org.

About the HMCC

Founded by leading members of the world's semiconductor community, the Hybrid Memory Cube Consortium (HMCC) is dedicated to the development and establishment of an industry-standard interface specification for the Hybrid Memory Cube technology. Members of the consortium include Altera Corporation, ARM, HP, IBM, Micron Technology, Open-Silicon, Inc., Samsung Electronics Co., Ltd., SK hynix Inc., and Xilinx, Inc. To learn more about the HMCC, visit www.hybridmemorycube.org.

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