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The Way Forward for Electronic Design
by Steve Leibson

3D Thursday: Hybrid Memory Cube—wide I/O only more so—gets an industry consortiu

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Back in August, I wrote about the 3D SDRAM assembly called the Micron Hybrid Memory Cube (HMC, see "Want to know more about the Micron Hybrid Memory Cube (HMC)? How about its terabit/sec data rate?") and I called it a "killer app" for 3D IC assembly. Last week, founding members Micron and Samsung announced the Hybrid Memory Cube Consortium (HMCC) dedicated to expandi capabilities of the next generation of memory-based solutions." Current "Developer Member" compani include Altera, Micron, Open-Silicon, Samsung, and Xilinx. Although the technology scales down mem goals of the group are not scaled down at all:

"With performance levels that break through the memory wall, Hybrid Memory Cube represents the ke extending network system performance to push through the challenges of new 100G and 400G infrastr growth. Eventually, HMC will drive exascale CPU system performance growth for next generation HPC systems."

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