

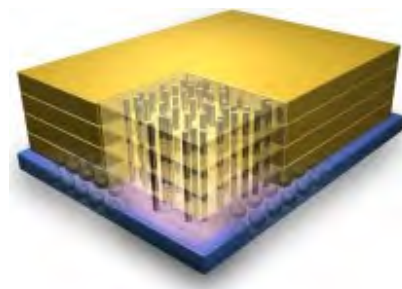
Microsoft to Support Hybrid Memory Cube Technology

Microsoft Joins Hybrid Memory Cube Consortium

by [Anton Shilov](#)

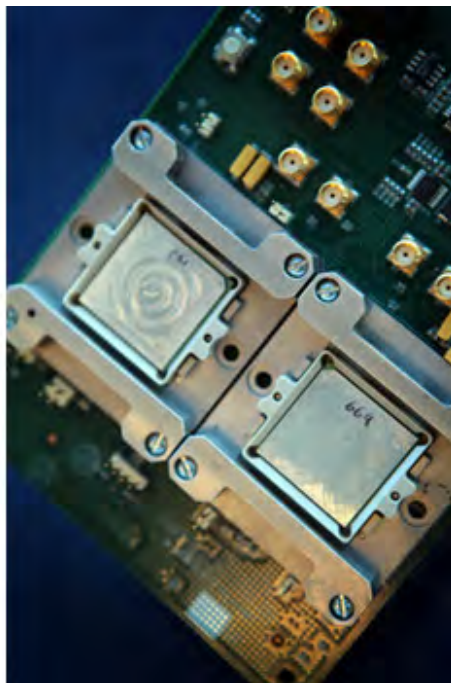
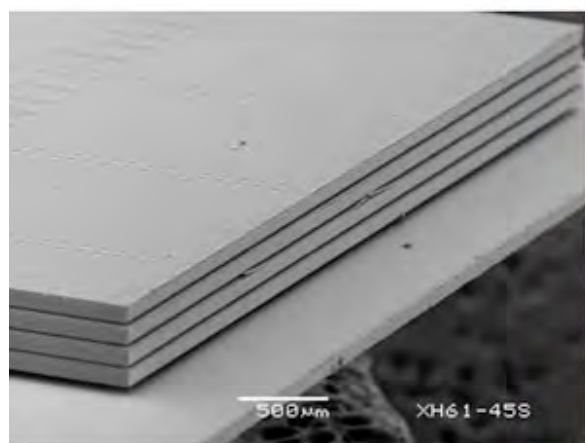
05/08/2012 | 08:26 PM

The Hybrid Memory Cube Consortium, led by Micron Technology and Samsung Electronics, on Tuesday said that Microsoft Corp. has joined the consortium. The HMCC is a alliance of equipment makers, enablers and integrators cooperating to develop and implement an open interface standard for new memory technology called the hybrid memory cube. It is unknown whether Microsoft will implement HMC into its Xbox Next, or will just support the tech by Windows operating systems.



"HMC technology represents a major step forward in the direction of increasing memory bandwidth and performance, while decreasing the energy and latency needed for moving data between the memory arrays and the processor cores. Harvesting this solution for various future systems could lead to better and/or novel digital experiences," said KD Hallman, general manager of Microsoft strategic software/silicon architectures.

Micron and Samsung, the initial developing members of the HMCC, are working closely with Altera, IBM, Open-Silicon, Xilinx and now Microsoft to accelerate widespread industry adoption of HMC technology. The technology will enable highly efficient memory solutions for applications ranging from industrial products to high-performance computing and large-scale networking. The HMCC's team of developers plans to deliver a draft interface specification to a growing number of "adopters" that are joining the consortium. Then, the combined team of developers and adopters will refine the draft and release a final interface specification at the end of this year.



One of the primary challenges facing the industry – and a key motivation for forming the HMCC – is that the memory bandwidth required by high-performance computers and next-generation networking equipment has increased beyond what conventional memory architectures can provide. The term “memory wall” has been used to describe the problem.

Breaking through the memory wall requires a new architecture that can provide increased density and bandwidth at significantly reduced power consumption. HMC capabilities are a leap beyond current and near-term memory architectures in the areas of performance, packaging and design efficiencies. By defining an industry interface specification for developers, manufacturers and architects, the consortium is committed to making HMC a successful new high-performance memory technology.

Intel Corp. demonstrated HMC at Intel Developer Forum in September, 2011. The Hybrid Memory Cube – which was jointly designed by Intel and Micron – demonstrates a new approach to memory design delivering a 7-fold improvement in energy-efficiency over today's DDR3. Hybrid Memory Cube uses a stacked memory chip configuration, forming a compact “cube”, and uses a new, highly efficient memory interface which sets the bar for energy consumed per bit transferred while supporting data rates of 1Tb/s (one trillion bits per second). This research technology could lead to dramatic improvements in servers optimized for cloud computing as well as ultrabooks, televisions, tablets and smartphones.