Micron, Samsung, Hynix agree to 3-D memory spec

Rick Merritt

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The three top memory makers are among more than 100 companies releasing a specification for a 3-D DRAM and logic module called the Hybrid Memory Cube. SAN JOSE, Calif. – The Micron-led **Hybrid Memory Cube Consortium** has issued version 1.0 of its specification for a vertical memory stack with a defined logic-layer interface. Now the group will turn its focus to higher-speed variations of a dynamic random-access memory (DRAM) module stacked using through-silicon vias.

In its next-generation spec, the group aims to increase short-reach data rate across modules from the current 10, 12.5 and 15 Gbits/second up to 28 Gbits/s. Speeds for ultra-short reaches within a die will go from 10 Gbits/s today to 15 Gbits/s in the spec, which is expected to be complete by the first quarter of 2014.

The HMC group consists of more than 100 companies including Micron's rivals Samsung and SK Hynix as well as potential customers such as AMD, Cray, Fujitsu, IBM, Marvell, ST Microelectronics and Xilinx. Missing are big potential users including Intel and Nvidia.

Last year, a top Nvidia technical exec said the graphics chip company doesn't want a memory cube with a logic layer, although it is pursing 3-D ICs. So far, Micron insists the logic interface is required to hit its target data rates and bandwidth. "The logic also ensures resiliency and repair-ability in the field," said a spokesman for group.

Previously, Micron said it will deliver 2- and 4-Gbyte versions of the stack before June. They will provide aggregate bi-directional bandwidth of up to 160 Gbytes/second. The top three memory makers expressed support for the spec in a press statement.

"The consensus we have among major memory companies and many others in the industry will contribute significantly to the launch of this promising technology." said Jim Elliott, vice president of memory planning and product marketing at Samsung Semiconductor, Inc.

"HMC brings a new level of capability to memory that provides exponential performance and efficiency gains that will redefine the future of memory," said JH Oh, vice president of the DRAM product planning and enabling group at SK Hynix Inc.

"The industry agreement is going to help drive the fastest possible adoption of the HMC technology, resulting in what we believe will be radical improvements to computing systems and, ultimately, consumer applications," said Robert Feurle, Micron's vice president for DRAM marketing.

Separately, the **Jedec** standards effort is said to be working on a high-bandwidth memory interface as a follow on to its existing Wide I/O memory interface standard. Jedec does not comment on standards in progress.

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